Electromagnetic Compatibility Design Considerations

for

ISDN Terminal Equipment

Advanced Micro Devices
ISDN Systems Engineering

ISDN Terminal Equipment often contains high speed digital circuitry as well as a communications interface to an external bus. While these external bus signals are usually not sources of radiated emissions, the internal digital signals can generate emission levels greater than permitted. Background of how these emissions are generated is presented, as well as measures that can be used to reduce emission levels.

Introduction

Todays electronic system designers need to do more than just make their systems operate under ideal conditions in the development laboratory. Besides that obvious task, they must also make sure that the system will operate in the "real world". This requires that the system should not be affected by other equipment nearby (susceptibility), and should not itself be a source of interference to other equipment (emission). Electromagnetic Compatibility (EMC) must, therefore, be a major design objective.

A digital system is a radio-frequency (RF) system. Although most digital designers are knowledgeable about the subject of digital design, they are not always well-equipped to handle the design and analysis of RF systems. Recognizing the interference potential of digital electronics, the Federal Communications Commission (FCC), in 1979, imposed regulations that limit the emissions from digital electronics marketed in the United States. Similar regulations exist in other countries, such as the International Special Committee on Radio Interference (CISPR) standards used in Europe.

Even if a product functions properly, the possibility exists that it may not be legally marketed because of emission problems. Therefore, it is important to consider noise and emission control during the early design and layout stages of a product.

With the advent of ISDN, new Terminal Equipment is being developed for customer premises applications. Therefore, this application note is provided to give guidance on the design and layout of such systems to minimize the noise and emission produced.

Types of EMI Emission

Emission from digital electronic circuitry can occur as either differential mode or common mode. Differential mode emission results from high frequency current flowing around a circuit loop, which becomes an equivalent loop antenna. Emissions are produced by the magnetic fields from this current. Common mode emission occurs when a point in the circuit, which is the reference point for an external connection, becomes elevated from the circuit's ground due to undesired voltage drops in return paths. This elevated voltage produces current into this external connection, which becomes an equivalent monopole antenna. A representation of common mode and

differential mode emissions is shown in Figure 1.

Component Placement and Board Layout

The layout of a printed wiring board starts with the placement of the components on the board. Time spent at this point, on the EMC implications of the layout, can significantly reduce the noise and emissions from the board. Components should be laid out to minimize the length of high frequency signal runs, especially clocks.

Cables that leave the board should be located in a separate I/O area of the board to minimize the noise coupling from other components. Components needed to minimize common-mode currents on the cables should be located at the perimeter of the I/O area. No traces, other than those for the cables, should be located in the I/O area. Clocks and other high frequency digital circuitry should be kept away from the I/O area.

Separate areas of the board should be used for the analog and the digital circuits. Components that have both an analog and digital function should be placed along the dividing line between the two sections.

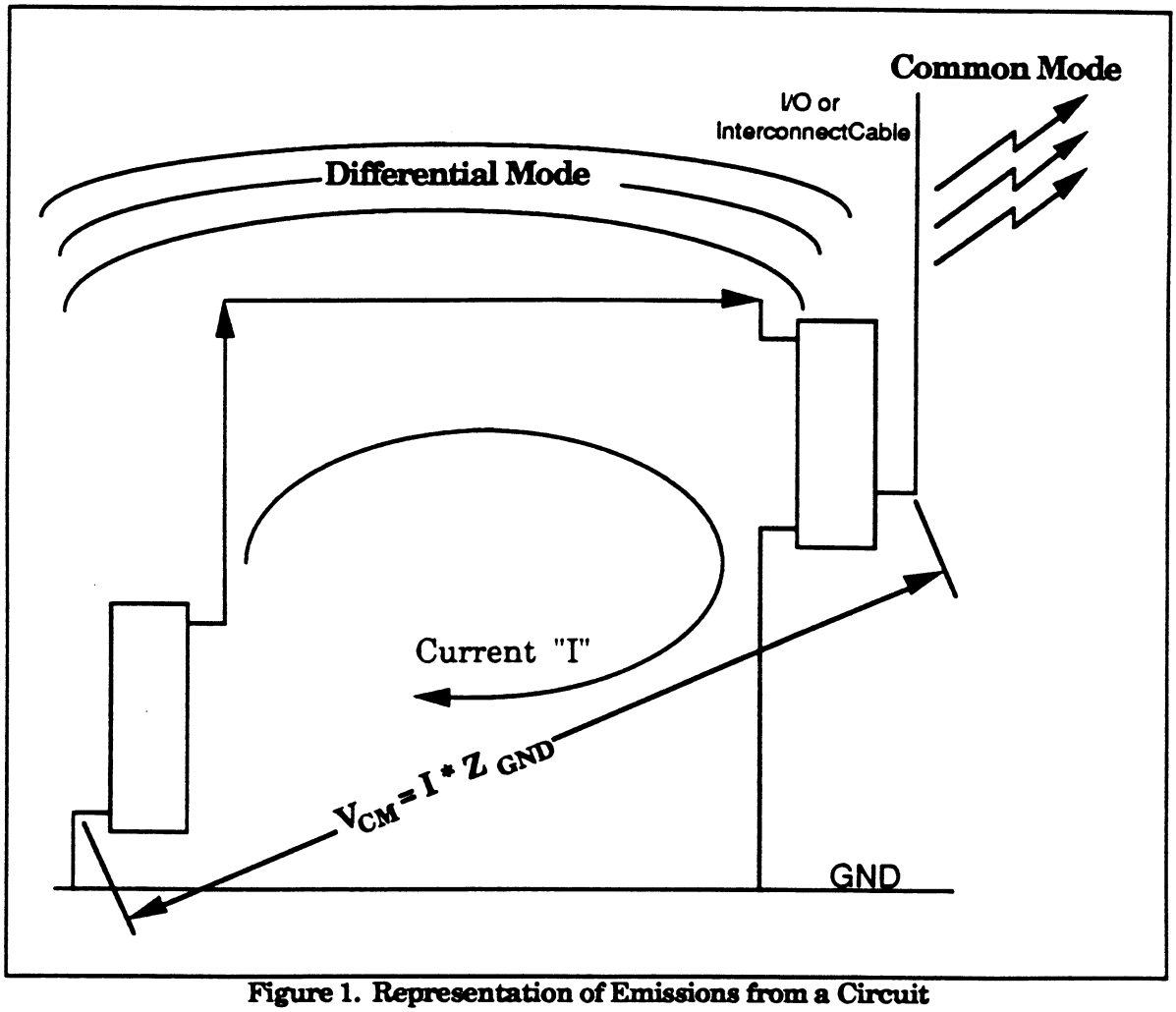


Figure 1. Representation of Emissions from a Circuit

Table 1.
Impedance of a 1" Long Printed Wiring Board Trace.

Frequency (MHz)	Rise Time (nS)	Impedance (ohms)
16	20	1.5
32	10	3.0
64	5	6.0
80	4	7.5
106	3	10.0
160	2	15.0
320	1	30.0

Grounding and V_{CC} Routing

The ground system on a high-speed digital logic board must provide a low-impedance connection between all possible combination of points that communicate with each other. This minimizes the ground noise voltage generated. The ground noise voltage is produced by both transient power supply currents and signal return currents. The power supply transients can be controlled by proper use of decoupling capacitors, but the signal return currents in the ground cannot be decoupled or bypassed.

Ground noise voltage can be a major cause of functional problems as well as being the driving function for radiated emission from the board. A typical printed wiring board trace (0.02" wide) has a resistance of 12 milliohms/inch and an inductance of 15 nH/inch. The impedance of 15 nH of inductance versus frequency (which is also related to the pulse rise and fall time by the Fourier Series) is shown in Table 1. For a digital signal with a 2 nS rise time, the ground conductor will have an inductive reactance of 15 ohms/inch. Therefore, the inductive reactance of the trace is much greater than the 12 milliohm/inch trace resistance.

It is the trace inductance that is of most concern when laying out a printed wiring board ground system. The impedance must be reduced by an order of magnitude or more from the values shown in Table 1. The most practical way to do this is to provide many alternative (parallel) paths for the ground current. One way to accomplish this is by the use of a ground plane. Although a ground plane will produce optimum performance, its use may not be desirable because of the expense associated with a multilayer board.

In the absence of a ground plane, the layout of the ground traces is critical to the EMC performance of the circuit. An almost equally effective method of reducing inductance is to use a gridded ground system.[1,2] An acceptable grid size would be a spacing of 0.5", although good performance can often be obtained with much larger spacings. A good rule to follow is to start with a grid size whose spacing falls between every IC on the board, then after all the other traces have been routed, fill in the grid as much as possible.

Although wide ground traces are desirable to handle the DC current, without a large voltage drop, they do not necessarily control the ground noise. The ground noise is controlled by the lowered inductance produced by providing many parallel ground paths, not by the width of any one trace.

The V_{CC} power distribution system layout should be the same as, and parallel to, the ground system. If a ground plane is used, a power plane should also be used. Likewise, the user of a ground grid requires the addition of a power grid.

Decoupling

When most digital logic gates switch they draw a large transient current from the power supply. This transient current flowing through the inductance of the power supply traces produces a voltage drop across this inductance. The magnitude of this power supply transient can be reduced by decreasing the inductance, and/or decreasing the current flowing through the inductance. The transient current through the power supply traces can be minimized by supplying the current from another source, such as a capacitor near the IC. The noise voltage is now a function of the decoupling capacitor and the wiring between it and the IC. The type of capacitor used, its value, and placement are all important considerations in determining the capacitor's effectiveness. Typically a 0.01 to 0.1 μF multilayer ceramic capacitor placed as close as possible to the power and ground pins of the IC is used. It is very important that the loop area (inductance) between the decoupling capacitor and the IC is minimized. A properly placed decoupling capacitor solves two problems: 1) The capacitor minimizes the noise voltage generated on the V_{cc} bus; and 2) It provides a much smaller loop area for the high-frequency transient power supply current to flow in, thus minimizing the radiation.

In addition to the individual IC decoupling capacitors, a bulk decoupling capacitor is also required to recharge the individual capacitors. Whereas the individual decoupling capacitors must operate at frequencies determined by the switching speed of the ICs, the bulk decoupling capacitor only has to operate at the clock frequency. A good rule for the value of the bulk decoupling capacitor is ten times the sum of all the individual decoupling capacitors. The bulk decoupling capacitor should be located where power comes onto the board.

Crystal Oscillator and Clocks

Crystal oscillator board layout is critical. The crystal should be placed as close to the IC oscillator pins as possible. The two traces between the crystal and the IC should be run so as to form the minimum loop area possible. The traces between the crystal and the oscillator load capacitors should also have the smallest loop area possible. The trace between the load capacitor ground and the IC ground must also be kept as short as possible.

A clock output from any device should be routed with an adjacent ground trace. Both the clock and ground traces should be as short as possible. The adjacent ground trace should be routed as close as absolutely possible to the entire clock trace and terminate at both ends to ground connections of both the source and destination devices, to provide a minimum loop area. A suggested layout for crystal oscillator and clock signals is shown in Figure 2.

Frequency

Radiation from a digital system is proportional to frequency or frequency squared, according to the mechanism involved.[2] This is shown in equations 3 and 4. Therefore it is desirable to limit the frequency and rise time of signals to those required for functionality. The rise time is important since it determines the harmonic content of the signal. Resistors or small ferrite beads can be placed in series with high frequency clock leads in order to slow down the rise time, as permitted by minimum edge requirements of devices receiving the clock.

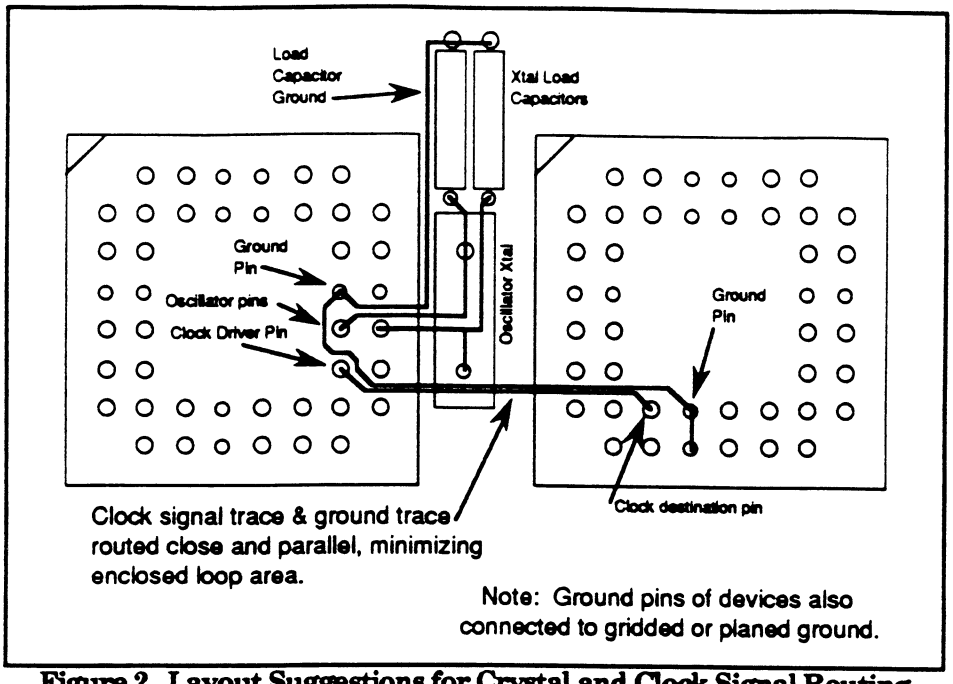


Figure 2. Layout Suggestions for Crystal and Clock Signal Routing

Cables

Noise voltages generated on the printed wiring board (such as the ground noise voltage) will act as a source to drive a common-mode current out on any cables connected to the board, thus causing them to radiate. The amount of common-mode current required on a cable to exceed the FCC emission limit is only a few microamps.[2] Therefore, depending on the magnitude of this ground noise at the location where external connections are made, all cables leaving the board at this area may require treatment to reduce this common-mode current. On non ground-plane boards another source of common-mode current is an asymmetrical dipole antenna formed by the traces, and driven by the signal voltages.[3]

The key to controlling common-mode radiation from cables is to minimize the common-mode current in the cables. The common-mode current can be minimized by:

1. Minimizing the ground noise voltage that is the source of the common-mode current on the cables.
2. Add a high common-mode impedance (choke) in series with the cable.
3. Divert the common-mode current (shunt capacitor) so it does not flow on the cable.
4. Shield the cable to prevent the common-mode current from radiating.

The first step in controlling the common-mode radiation is to minimize the ground noise voltage that drives the cable. This can be done by the use of a ground plane or grid as discussed above. This by itself, however, may not be sufficient and some additional suppression of the common-mode current may be required.

A common-mode choke[2] can provide a high impedance to the common-mode cable current without affecting the

differential-mode signal current. Such a choke consists of two or more windings on a ferrite core. The effectiveness of a common-mode choke is normally limited to less than 20 dB because of the bypassing effect of the choke's parasitic capacitance.

Cables acting as common-mode antennas typically have driving point impedances of several hundred ohms. To be effective, a common-mode choke must provide an impedance that is significantly greater by comparison. Therefore common-mode chokes must have impedances in the range of five to six hundred ohms at the frequency of interest to be effective.

Cable decoupling (shunting the noise current to ground) and cable shielding both require a "quiet" or "clean" ground (one not contaminated by the digital logic noise). The ground that the noise is shunted to is usually the chassis or a separate image plane.[3] A small capacitor (typically a few hundred picofarads) is placed between each of the cable conductors and the "quiet ground". Both the ground and the signal conductors in the cable must be decoupled. The effectiveness of the cable decoupling capacitors depends on the common-mode impedance of the noise source. Sometimes better results can be obtained by using a series resistor or inductor in addition to the cable decoupling capacitor. Filtered pin connectors with built-in shunt capacitors can also be used if the shell of the connector is mounted to the chassis.

The common-mode suppression components used must be such that they affect the common-mode noise current (usually the clock harmonics) but not the differential-mode signal currents on the cable. Since the interface cables normally carry lower frequency signals than the clock harmonics, this is usually easy to achieve.

Relationship of Rise and Fall Times to Radiated Emission Spectrum

A repetitive digital signal is typically represented by a square wave, although in reality it more closely resembles a trapezoidal wave, with finite rise and fall times. Such a signal is actually made up of a fundamental frequency, plus many harmonic components. Even if this fundamental frequency is low enough to not be a concern within the regulated emissions spectrum, its harmonics typically are of concern. The magnitude of these harmonics is related to the overall signal wave shape and especially to the edge rise times. Assuming identical rise and fall times, the Fourier component magnitudes of a periodic signal of period T are described by Equation 1.

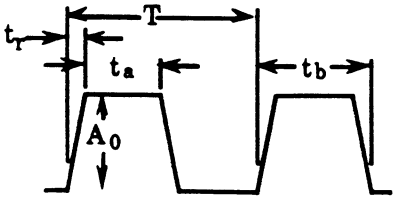
$$A_n = A_0\left(2\,\frac{t_r + t_a}{T}\right)\left|\frac{\text{SIN } n\pi\,\frac{t_r}{T}}{n\pi\,\frac{t_r}{T}}\right|\left|\frac{\text{SIN } n\pi\,\frac{t_r + t_a}{T}}{n\pi\,\frac{t_r + t_a}{T}}\right| \quad \text{for } n = 1 \text{ to } \infty \qquad \text{(Eq. 1)}$$

Where:

T = Period = $\frac{1}{f}$ $\quad t_r$ = Rise Time = $\frac{t_b - t_a}{2}$

d = duty cycle = $\frac{t_r + t_a}{T}$

A_0 = peak-to-peak signal amplitude



For a symmetrical signal, the duty cycle, d becomes 0.5 and Eq. 1 simplifies to:

$$A_n = A_0 \left| \frac{\text{SIN } n\pi\frac{t_r}{T}}{n\pi\frac{t_r}{T}} \right| \left| \frac{\text{SIN } \frac{1}{2} n\pi}{\frac{1}{2} n\pi} \right|$$

(Eq. 2)

In comparing the magnitudes of each harmonic component as the rise time varies, the spectrum envelope outlining these magnitudes decreases at a rate of -20 dB per decade, from the fundamental frequency up to a frequency of $f = 1/\pi t_r$. Thereafter, it decreases at a rate of -40 dB per decade. For example, the spectrum envelope breakpoint frequency for a 16 MHz signal with 2 ns rise times is 159 MHz. At frequencies beyond this point, the magnitudes decrease at -40 dB per decade. If the edge is slowed to 6 ns, this breakpoint occurs at 53 MHz. By slowing the rise time, the spectral components now begin a faster decrease in amplitude (-40dB/decade), starting at a lower initial breakpoint frequency.

Equation 2 can be used to determine the relative differences of harmonic components of a clock signal. By combining the individual frequency contributions with Equations 3 and 4, an estimate of expected emission levels can be calculated. If there is freedom to slow a clock edge in a design, the expected reduction of emission levels can also be determined.

Electric Field Measurement from Differential Mode Emissions

Differential mode emissions emanate from current flowing around a circuit loop. If the loop perimeter is less than one quarter of the wavelength, the magnitude of the electric field in volts per meter from this equivalent antenna can be approximated by:

$$E = 2\left(1.31 \times 10^{-14} \right)\left(\frac{f^2 A I}{r}\right)$$

(Eq. 3)

where:

- A = Loop area in square meters
- I = Current in amps through the loop
- r = Distance in meters of electric field measurement
- f = Frequency in Hertz of the contributing current element

The factor of 2 is included to account for the extra ground reflection of measurement made over a reflecting ground plane, a requirement of most regulations. For a 6 ma signal of 48 MHz travelling through a 35 square cm area loop, the measured electric field at 10 meters is 126 microvolts per meter, which is above the maximum permitted by FCC Class A requirements of 90 microvolts per meter. By routing a parallel ground return path the loop area could easily be reduced, which would reduce the emission level.

The squaring of frequency in Equation 3 causes emission levels to increase at a rate of +40dB per decade. Superimposing this increase of emissions with the decreasing levels of harmonic components (from Eq. 2), the net emission level increases at +20 dB per decade. When the frequency equals the breakpoint of $f=1/\pi t_r$, the harmonic magnitude now decreases at the same rate the frequency squared emission contribution increases, and the overall emission level becomes flat with frequency. The obvious conclusion is that differential mode emission levels can be minimized by limiting the rise times of the signal in order to more quickly flatten out the amplitude increases from increasing harmonic frequencies.

Electric Field Measurement from Common Mode Emissions

Common mode emissions result from current driven into an equivalent antenna (connecting cable, etc.) which is

connected to a point in the circuit that is electrically elevated above ground. For such an equivalent monopole antenna, the magnitude of the electric field in volts per meter can be approximated by:

$$E = 1.26 \times 10^{-6} \cdot \frac{fIL}{r}$$

(Eq. 4)

where:

- f = Frequency in Hertz
- I = Current in amps into the antenna of length L meters
- r = Distance in meters of electric field measurement

For a circuit having a ground return path of 10 centimeters, at 80 MHz the impedance would be (at 5.9 nH/cm trace inductance) 3 ohms. A current of 2 milliamps at this frequency will produce a voltage drop of 6 millivolts. At a nominal driving point impedance for a 1 meter long cable of approximately 300 ohms, the net current into this "antenna" would be 20 microamps. From Eq 4, the electric field measured at a distance of 10 meters would be 202 microvolts per meter. This is above the maximum FCC Class A emission level requirement of 90 microvolts per meter. It becomes quite clear that the ground return path impedance can be very significant in contributing to – or controlling – emission levels.

Emission from this source increases linearly with frequency at +20 dB per decade. Again superimposing this increase of emissions with the decreasing levels of harmonic components (from Eq. 2), the net emission level remains flat up to the $f=1/\pi t_r$ breakpoint, and then begins to decrease at -20 dB per decade.

Summary

Attention to EMC issues early in the design can minimize the cost of dealing with EMC problems later in the development cycle. Early board level EMC considerations are the most cost effective approach to achieving compliance with regulations. Board layout, component selection, circuit design, and an understanding of basic EMC principles all play an important part. Key issues to be considered are:

- Minimize the loop area enclosed by all high frequency signals.
- Minimize the current drive capability and loading of a high frequency source and limit the rise times to as slow an edge as possible. If necessary add components to slow down excessively fast edges, especially if they must be routed long distances.
- Isolate external connecting cables to an electrically "clean" I/O area on the board and if necessary, add decoupling to external cables.
- Minimize power and ground return impedances with gridded networks or if possible, with power/ground planes.
- Provide good decoupling for noisy devices .
- Minimize signal trace length of oscillator and clock paths, and provide a closely-routed parallel return path.

References

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2. Ott, H. W., "Noise Reduction Techniques in Electronic Systems", Wiley, New York, 1988.
3. German, R. F., H. W. Ott, C. R. Paul, "Effect of an Image Plane on Printed Circuit Board Radiation", IEEE International Symposium on Electromagnetic Compatibility, 1990.

